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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,464	07/07/2003	Jian-Shen Yu	B-5152 621073-4	9339

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/615,464	YU, JIAN-SHEN
	Examiner	Art Unit
	Daniel D. Chang	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed February 28, 2005.

Claim Objections

Claims 19 and 20 are objected to because of the following informalities: Claim 19, line 3, "the disable signal" appears to be --a disable signal--. Claim 20, line 2, "the source" appears to be --a source--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 9-11, and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima et al. (US 6,664,943 B1).

Regarding claim 1, Nakajima discloses, at least in Fig. 11, a level-shifting circuit comprising:

a level modulating circuit having an input terminal (in1) and an inverse input terminal (in2) for respectively receiving a complementary pair of small signals, and a first output terminal (2) for outputting a voltage level in response to the complementary pair of small signals; and

an enable circuit (Qn13, Qn14, Qp13, Qp14) coupled to the first output terminal and making the first output terminal output a predetermined voltage level signal (output state of 71 or 72) when receiving a disable signal (when CNTL=LOW).

Regarding claim 2, Nakajima discloses, at least in Fig. 11, that the enable circuit is a MOS transistor (Qp14) having a source and a drain coupled between an external level (VDD) and the first output terminal (2) and a gate coupled to the disable signal (CNTL).

Regarding claim 3, Nakajima discloses, at least in Fig. 11, that the enable circuit is a first PMOS transistor (Qp14) having the source coupled to a power source, and the drain coupled to the first output terminal.

Regarding claim 5, Nakajima discloses, at least in Fig. 11, that the enable circuit further comprises a pair of second NMOS transistors (Qn13, Qn14) having drains respectively coupled to the input terminal and the inverse input terminal, sources coupled to the complementary pair of small signals, and gates coupled to the disable signal.

Claims 9-11 and 13-14 are essentially the same in scope as apparatus claims 1-3 and 5, and are rejected similarly.

Regarding claim 15, Nakajima discloses, at least in Fig. 11, that the enable circuit further comprises an inverter (79) coupled between the gates of the first N-type thin film transistor and the third N-type thin film NMOS transistor.

Regarding claims 16 and 17, Nakajima discloses, at least in Fig. 11, that said predetermined voltage level signal is fixed (when Qn13, Qn14, Qp13, Qp14 are OFF; CNTL=Low).

Claims 18-20 are essentially the same in scope as apparatus claims 1-3 and 5, and are rejected similarly with teachings of Fig. 11. Furthermore, Claims 18-20 are also rejected with teachings of Figs. 12 and 13 as follows:

Regarding claim 18, Nakajima discloses, in Figs. 12 and 13, a level-shifting circuit, comprising:

a level modulating circuit having an input terminal (in1) and an inverse input terminal (in2) for respectively receiving a complementary pair of signals, and a first output terminal (2) for outputting a first voltage level in response to the complementary pair of signals; and

an enable circuit (Qp15) coupled to the first output terminal to cause the first output terminal to output a second voltage level signal (when RESET; see Fig. 13) independent of the first voltage level.

Regarding claim 19, Nakajima discloses, in Figs. 12 and 13, that the enable circuit is a MOS transistor (Qp15) having a source and a drain coupled between an external level (VDD) and the first output terminal, and a gate coupled to a disable signal (82).

Regarding claim 20, Nakajima discloses, in Figs. 12 and 13, that the enable circuit is a PMOS transistor (Qp15) having a source coupled to a power source (VDD), and the drain coupled to the first output terminal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6-8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (US 5,387,828) in view of Terletzki (US 6,501,298 B1).

Nakano teaches all the features of the claimed invention, with the exception of teaching the claimed enable circuit.

Terletzki teaches enable circuit (inverter 20 and transistors N1 and N3 in Fig. 2) that is coupled to the level shifting section and is responsive to an enable/disable signal for driving the output terminal of the level-shifting section to a predetermined voltage level during a disable mode.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the level shifter of Nakano with the enable circuit as taught by Terletzki in order to provide a predetermined voltage level during a disable mode.

Regarding claim 12, as for the "thin film transistor", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments filed 2/28/2005 have been fully considered but they are not persuasive.

Applicant argues on page 8 of the Amendment filed 2/28/2005, that "'the enable circuit' recited in Claim 1 [also Claim 9] is not disclosed by the transistors Qp13, Qn13, Qp14, Qn14,

because these transistors perform as resistors that play an integral part in shifting the voltage levels of the inputs 'in1' and 'in2'' to the power supply VDD amplitude output signals 'out', 'xout'". However, Nakajima discloses in col. 17, lines 47+, that "the NMOS transistors Q[n]13, Q[n]14 and the PMOS transistors Qp13, Qp14 are switched by means of a control signal CNTL.... In this way, a structure is obtained for switching the transistors Qn13, Qn14, Qp13, Qp14 in the CMOS latch cell 70 by means of the control signal CNTL and set to an active level only when a level shift is required in this level shift circuit, and the data held or in other words, the logic status of the input signal in1, in2 held when a level shift is not required, thereby achieving a combination latch and level shift circuit." Therefore, the transistors Qp13, Qn13, Qp14, Qn14 are interpreted as "the enable circuit".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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dc

DANIEL CHANG
PRIMARY EXAMINER